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09/808339
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ISSUE CLASSIFICATION	
Class	Subclass

<div>mt</div> <div>O.I.P.E.</div> <div>82</div> <div>SCANNED</div> <div>G.A.</div> <div>hr</div>	PATENT DATE
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APPLICATION NO 09/808339	CONT/PRIOR D	CLASS 706 703	SUBCLASS 14	ART UNIT 2122 2105	EXAMINER PHAN, THAI
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TITLE	APPLICANTS
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System and method for simulation of an integrated circuit design using a hierarchical input netlist and divisions along hierarchical boundaries thereof

PTO-2040
12/89[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input checked="" type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner)		NOTICE OF ALLOWANCE MAILED _____	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____	_____ (Primary Examiner)		ISSUE FEE Amount Due Date Paid	
<input type="checkbox"/> The terminal ____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)		ISSUE BATCH NUMBER _____	

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